A hardware-efficient neural network processor for deep neural network model learning is designed using a 1.12×0.86mm² 65nm CMOS process. The processor is composed of three main parts: (a) the ARM Cortex-A72 core, (b) the neural network accelerator, and (c) the memory controller. The processor can be powered by a 3.3V/1.2V regulator and is able to support single-precision floating-point arithmetic operations. The processor can achieve a peak performance of 8TOPS at 1.2V/96.9ns and 1.6TOPS at 1.8V/97.4ns. The processor can be used in various applications such as computer vision, speech recognition, and natural language processing.

Figure 3.1: The proposed hardware-efficient neural network processor.

This processor achieves a high level of efficiency by using a novel architecture that reduces the number of operations required for neural network computations. The architecture includes a dedicated layer for matrix operations, which results in a significant reduction in power consumption and latency compared to traditional processors. The processor is also designed to support mixed-precision arithmetic, allowing it to be used in a wide range of applications with varying requirements.

Figure 3.2: The architecture of the proposed processor.

The processor is designed to be easily integrated into existing systems, with minimal impact on the system's overall performance. It can be used as a standalone unit or in combination with other hardware components to create a powerful system for deep learning.

Figure 3.3: The system integration of the proposed processor.

The processor is designed to be compatible with existing deep learning frameworks, allowing it to be used in a variety of applications. It is also designed to be easily programmed, allowing developers to quickly create and deploy new models.

Figure 3.4: The software development environment for the proposed processor.

The processor is designed to be easily programmable, allowing developers to quickly create and deploy new models. It is also designed to be easily integrated into existing systems, with minimal impact on the system's overall performance.

Figure 3.5: The integration of the proposed processor into an existing system.
Such scenarios occur for example in office environments with strong reflections. In 40nm CMOS we achieve maximum data rates for SC-QPSK, OFDM-64QAM, and FBMC-64QAM of 7Gbps, 14Gbps, and 27Gbps, respectively. The spectrum efficiency of FBMC is 27% higher than OFDM.

The design for PPN FBMC-OQAM is based on a filter-bank, channel equalizer, high throughput FFT and phase noise cancellation (PNC). In order to achieve these requirements, the design is implemented in an 8T SRAM technology, which allows for a high degree of flexibility and fast switching times. The core area of the digital controller, DCO, and LDO are 0.00884 mm², 0.00325 mm², and 0.00312 mm², respectively.

Universal Sub-mW multi-phase Fast-Locking/GHz Cell-based ADPLLs

Figure 81-1 shows the layout of the ADPLL chip, which has been designed for applications requiring high-speed and high-frequency operation. The chip is composed of multiple sub-blocks, including a filter-bank, channel equalizer, high throughput FFT, and phase noise cancellation (PNC) stages. The layout is optimized for minimum power consumption and maximum performance.

The ADPLL is designed to support multiple operating frequencies, allowing for flexibility in different applications. The layout has been carefully designed to minimize parasitic effects and ensure accurate phase-locking across a wide range of frequencies. The chip is manufactured using a 16nm process technology, which provides excellent performance in high-speed applications.